CLAIMS

1. A digital filtering apparatus for use with a data signal line, comprising:

a digital delay element that receives data from a data signal line, the digital delay element having at least one output;

a comparator operably connected to the at least one output of the digital delay element, the comparator having an output; and

a final stage operably connected to the output of the digital delay element and the output of the comparator,

wherein the comparator, upon recognizing invalid data clocking through the digital delay element, enables the final stage to filter the data and wherein the comparator upon recognizing valid data clocking through the digital delay element, enables the final stage wherein the output of the final stage changes logical state for a duration approximately equal to that of the valid data.

2. The apparatus as recited in claim 1, wherein the digital delay element further comprises a plurality of shift registers operably connected in series.

3. The apparatus as recited in claim 1, wherein the digital delay element further comprises a plurality of flip-flops operably connected in series.

4. The apparatus as recited in claim 1, wherein the final stage further comprises a latch.

5. The apparatus as recited in claim 1, wherein the digital delay element has a clock cycle setting, and wherein invalid data comprises data that has changed logical state for a duration greater than the clock cycle setting.

6. The apparatus as recited in claim 1, wherein the digital delay element further comprises a plurality of digital delay elements operably connected in

series, and wherein the bandwidth of the filter is increased by increasing the number of digital delay elements operably connected in series and the bandwidth of the filter is decreased by decreasing the number of digital delay elements operably connected in series.

7. The apparatus as recited in claim 1, wherein the digital delay element has a plurality of output lines, wherein the comparator has a plurality of programmable input lines connected to the plurality of output lines of the digital delay element, and wherein the bandwidth of the filter is established by the number of comparator output lines that are programmed to receive data from the digital delay element.

8. A method for digitally filtering invalid data from a data signal line, comprising:

delaying with a digital delay element data from the data signal line;

determining with a comparator valid data clocking through the digital delay element; and

transitioning logical data states of an output line in response to the comparator recognizing valid data, wherein the duration of the logical data state transition is approximately equal to the duration of the valid data.

9. The method as recited in claim 8, wherein the output line further comprises a final stage latch connected to the comparator, and wherein the transitioning step further comprises enabling the final stage latch.

10. The method as recited in claim 8, wherein the digital delay element further comprises a plurality of flip-flops connected in series, and wherein the delaying step further comprises clocking data from the data signal line through the plurality of flip-flops.

11. The method as recited in claim 10, wherein the filtering method has a bandwidth, and wherein the filtering method further comprises the step of adjusting the bandwidth of the filtering method by increasing or decreasing the number of flip-flops in the digital delay element.

12. The method as recited in claim 8, wherein the filtering method has a bandwidth, wherein the comparator has a plurality of programmable input lines connected to the digital delay element, and wherein the filtering method further comprises the step of adjusting the bandwidth of the filtering method by adjusting the number of the plurality of programmable input lines that can receive data from the digital delay element.